Remarks/Arguments:

Applicants' disclosure is directed to a gate driver for forcing a power transistor having a gate electrode to either conduct or shut off. The gate driver includes a first current source and a second current source. The first current source outputs a first current that lowers the electric potential of the gate electrode and causes the power transistor to begin conducting The second current source outputs a second current that raises the electric potential of the gate electrode and causes the power transistor to shut off.

Claim 1 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Lewis (U.S. Patent No. 4,797,579). Claim 3 stands rejected under 35 U.S.C. § 103(a) as obvious over Lewis and Hsaio et al. (U.S. Patent No. 6,437,611). Claim 5 stands rejected under 35 U.S.C. § 103(a) as anticipated by Lewis and Kogushi (U.S. Patent No. 6,236,239). It is respectfully submitted, however, that the claims are patentable over the art of record for the reasons set forth below.

Lewis is directed to a CMOS VLI driver with controller rise and fall times. The driver includes voltage generators 16 and 18. Generator 16 controls the rise time of an output signal Vo and generator 18 controls the fall time of output signal Vo.

Applicants' invention, as recited by claim 1, includes a feature which is neither disclosed nor suggested by the art of record, namely:

> ...a first current source configured to receive a first control signal and to output a first current value...the first current value depending on a level of the first control signal...
>
> ...a second current source configured to receive a second control signal and to output a second current value...the second current value depending on a further level of the second control signal...
>
> ...wherein the respective levels of the first control signal and the second control signal are independently controllable....

This feature is found in the originally filed application at page 13, lines 7-11. No new matter has been added.

Lewis discloses use of voltage generators 16 and 18. Generator 16 controls the rise time of an output signal Vo and generator 18 controls the fall time of output signal Vo. Generator 16, for example, includes P transistor 30 and N transistor 32 connected to form an unbalanced CMOS inverter. The inverter is unbalanced in the sense that the width length (W/L) ratio of P transistor 30 is "much greater" than the W/L ratio of N transistor 32. The different W/L ratios control "the relative magnitude of current passing through" transistors 30 and 32. Here, the P transistor has a higher W/L ratio than the N transistor and, therefore, the P transistor passes a greater magnitude of current than the N transistor. See col. 5, lines 28-45.

The Examiner equates P transistor 30 with Applicants' first current source and equates N transistor 32 with Applicants' second current source. However, the W/L ratios of the P and N transistors in Lewis determine the amount of current output by the respective P and N transistors. In Applicants' gate driver, on the other hand, the current output by the first and second current sources are controlled by the respective first and second control signals, as described in claim 1.

It is because Applicants include the feature of "a first current source configured to receive a first control signal and to output a first current value, the first current value depending on a level of the first control signal," "a second current source configured to receive a second control signal and to output a second current value...the second current value depending on a further level of the second control signal" and "the respective levels of the first control signal and the second control signal are independently controllable," that the following advantages are achieved. The gate driver is usable with power transistors having different output sizes and an appropriate speed of changing the power transistor from off to on and on to off may be achieved with a substantially small number of additional elements a lower cost.

Accordingly, for the reasons set forth above, claim 1 is patentable over the art of record.

Claims 3 and 5 include all the features of claim 1 from which they depend. Thus, claims 3 and 5 are patentable over the art of record for the reasons set forth above.

In view of the amendments and arguments set forth above, the above-identified application is in condition for allowance, which action is respectfully requested.

Respectfully submitted,

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